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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/760,309	01/21/2004	Tsang-Chi Kan	BHT-3111-404	1537

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EXAMINER	
DOAN, NGHIA M	
ART UNIT	**PAPER NUMBER**
2825	

DATE MAILED: 11/23/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/760,309	KAN ET AL.	
	Examiner	Art Unit	
	Nghia M. Doan	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *03* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01/21/2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-11* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-11* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *21 January 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Responsive communication application 10/760,309 filed on 01/1/2004, claims 1-11 are pending.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1-11 are rejected under 35 U.S.C. 102(e) as being anticipated by Kumagai (US PG Pub. 2003/00551218).

4. **With respect to claim 1**, Kumagai discloses an integrated circuit (IC) structure utilized in a standard cell, comprising:

a substrate including pluralities of circuit elements (cells) (pg. 1, ¶ 09); and

m metal layers (--wiring layers--), which are disposed on said substrate and utilized as connection layout for circuit elements, wherein each metal layer further including an isolation layer (-- insulating layer --) for electrical isolation among metal layers (pg. 2, ¶ 24; fig. 4 and pg. 3, ¶ 37);

said structure is characterized in that one terminal of at least one circuit element is arranged with a circuit passageway (-- penetrating/ passed through--), said circuit passageway extends (-- staked via --) from said substrate to n metal layers such that

any connection line in each metal layer can be connected with said terminal by said circuit passageway, wherein n is larger than 1 and n is less than m+1 (pg. 1, ¶ 09, 13, 19, 24, 46, 49, and claim 5).

5. **With respect to claim 2,** Kumagai discloses the IC structure of claim 1, wherein each circuit passageway connects through two metal layers (claim 2).

6. **With respect to claim 3,** Kumagai discloses the IC structure of claim 1, wherein each circuit passageway connects through three metal layers (claim 3).

7. **With respect to claim 4**, Kumagai discloses the IC structure of claim 1, wherein said circuit passageway can be formed by pluralities of metal layers and pluralities of vias (claim 8).

8. **With respect to claim 5**, Kumagai discloses the IC structure of claim 1, wherein said standard cell can be assembled as an intellectual property element (pg. 3, ¶ 37 and 40).

9. **With respect to claim 6,** Kumagai discloses the IC structure of claim 1, wherein said standard cell can be assembled as an intellectual property element library (pg. 1, ¶ 11 and pg. 3, ¶ 37 and 30).

10. **With respect to claim 7,** Kumagai discloses an integrated circuit (1C) layout design method utilized for connection of elements in a standard cell (fig. 1), wherein said IC comprises a substrate, said substrate further including pluralities of circuit elements (pg. 1, ¶ 9); and m metal layers (-- wiring layer--) disposed on said substrate, which are utilized as connection layout for circuit elements, wherein each metal layer further including an isolation layer for electrical isolation (-- insulating layer --) among

metal layers (pg. 2, ¶ 24; fig. 4 and pg. 3, ¶ 37) said IC layout design method comprising the following steps:

arranging a circuit passageway (-- penetrating/ passed through--) at one terminal of a circuit element, said circuit passageway extends (-- stacked via --) from said substrate through at least two metal layers (pg. 2, ¶ 16); and

connecting a line, which is required to be electrically connected to said terminal, to said terminal by connecting said line to said circuit passageway (pg. 2, ¶ 16).

11. **With respect to claim 8,** Kumagai discloses the IC layout design method of claim 7, wherein said circuit passageway connects through two metal layers (claim 2).

12. **With respect to claim 9,** Kumagai discloses the IC layout design method of claim 7, wherein said circuit passageway connects through three metal layers (claim 3).

13. **With respect to claim 10,** Kumagai discloses the IC layout design method of claim 7, wherein said standard cell can be connected to an intellectual property element (pg. 3, ¶ 37 and 40).

14. **With respect to claim 11,** Kumagai discloses the IC layout design method of claim 7, wherein said standard cell can be connected to an intellectual property element library (pg. 1, ¶ 11 and pg. 3, ¶37 and 30).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nghia M. Doan whose telephone number is 571-272-5973. The examiner can normally be reached on 8:30-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Smith can be reached on 571-272-1907. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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11/07/2005